1-27. (previously canceled)

28. (currently amended) An integrated circuit having a field-plated resistor the field-plated resistor comprising:

a. a resistor body formed in a semiconductor substrate, the resistor body having first and second contact regions,

b. a first insulating layer on the resistor body, the first insulating layer approximately coextensive with the resistor body and having a top surface and a bottom surface [, with the bottom surface in contact with the resistor body, and approximately coextensive therewith,]

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c. a contact window in the first insulating layer and extending from the top surface of the first insulating layer through the first insulating layer to the resistor body,

d. a field plate on the first insulating layer and approximately coextensive therewith and with the resistor body, the field plate having a top surface and a bottom surface, with a portion of the bottom surface extending through the contact window in the first insulating layer and into contact with the first contact region of the resistor,

e. a second insulating layer, with a first portion of the second insulating layer at least substantially covering the field plate,

f. an electrical contact to the top surface of the field plate,

g. an electrical contact to the second contact region of the resistor, and electrically insulated from the field plate, and

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h. a plurality of metal conductors formed on the first portion of the second insulating layer.

29. (previously added) The integrated circuit of claim 28 wherein the field plate comprises polysilicon.

30. (previously added) The integrated circuit of claim 29 wherein the first and second insulating layers are SiO_2.

31. (canceled)

32. (previously added) The integrated circuit of claim 29 further comprising an insulative spacer formed around the field plate.

33. (previously added) The integrated circuit of claim 29 wherein the electrical contact to the top surface of the field plate comprises a barrier layer.

34. (previously added) The integrated circuit of claim 33 wherein the electrical contact to the second contact region of the resistor comprises a barrier layer.

35. (currently amended) An integrated circuit having a field-plated resistor the field-plated resistor comprising:

a. a resistor body formed in a semiconductor substrate, the resistor body having first and second contact regions,

b. a first insulating layer on the resistor body, the first insulating layer approximately coextensive with the resistor body and having a top surface and a bottom surface [, with

the bottom surface in contact with the resistor body, and approximately coextensive therewith,]

c. a contact window in the first insulating layer and extending from the top surface of the first insulating layer through the first insulating layer to the resistor body,

d. a field plate on the first insulating layer and approximately coextensive therewith and with the resistor body, the field plate having a top surface and a bottom surface, with a portion of the bottom surface extending through the contact window in the first insulating layer and into contact with the first contact region of the resistor,

e. a second insulating layer, with a first portion of the second insulating layer at least substantially covering the field plate,

f. a metal layer comprising

i. an electrical contact to the top surface of the field plate,

ii. an electrical contact to the second contact region of the resistor, and electrically insulated from the field plate, and

iii. a plurality of metal conductors formed on the first portion of the second insulating layer.

36. (currently amended) A method for the manufacture of an integrated circuit having a field-plated resistor the field-plated resistor comprising:

a. forming a resistor body in a semiconductor substrate, the resistor body having first and second contact regions,

b. a first insulating layer on the resistor body, the first insulating layer approximately coextensive with the resistor body and having a top surface and a bottom surface [, with the bottom surface in contact with the resistor body, and approximately coextensive therewith,]

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c. forming a contact window in the first insulating layer and extending from the top surface of the first insulating layer through the first insulating layer to the resistor body,

d. forming a field plate on the first insulating layer and approximately coextensive therewith and with the resistor body, the field plate having a top surface and a bottom surface, with a portion of the bottom surface extending through the contact window in the first insulating layer and into contact with the first contact region of the resistor,

e. depositing a second insulating layer, with a first portion of the second insulating layer at least substantially covering the field plate,

f. depositing a metal layer,

g. patterning the metal layer to form

i. an electrical contact to the top surface of the field plate,

ii. an electrical contact to the second contact region of the resistor, and electrically insulated from the field plate, and

iii. a plurality of metal conductors formed on the first portion of the second insulating layer.

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37. (previously added) The method of claim 36 wherein the field plate comprises polysilicon.

38. (previously added) The method of claim 37 wherein the first and second insulating layers are SiO_2.

39. (previously added) The method of claim 38 further including the step of forming an insulative spacer formed around the field plate.